REMARKS

Claim Rejections 35 U.S.C. § 102 (b)

Claims 26-28

In the Office Action Summary dated April 14, 2004, the Examiner has indicated in the section of the form regarding disposition of claims that claims 24-26 were pending and that he has rejected them. However, the Examiner subsequently refers to claims 26-28 in his remarks. Applicant believes that the Examiner intended to reject claims 26-28 so Applicant will respond accordingly.

Furthermore, the Examiner has cited Tsuji (JP 08-204136), but refers to Kenji in his remarks. Applicant believes that the Examiner intended to refer to Tsuji (JP 08-204136) in his remarks so Applicant will respond accordingly below.

The Examiner has rejected claims 26-28 under 35 U.S.C. § 102 (b) as being anticipated by Tsuji (JP 08-204136).

Applicant respectfully disagrees with the Examiner. Applicant has amended claim 26. Claim 26, as amended, claims a device having I/O connections to a package or board including: vias; a bond pad disposed over the vias, the bond pad having two or more segments, wherein each of the segments is electrically connected to two or more of the vias, and a wire lead attached directly to the segments. See Figure 4 and Figure 5. Also, see lines 12-15 on page 10 of the specification.

In contrast, the Tsuji reference cited by the Examiner teaches a bond pad (2) of two or more segments (2a) with a wire lead (6) directly attached. See Figure 2 (a) and Figure 2 (d). However, Tsuji fails to teach that each of the segments is electrically connected to two or more of the vias. Thus, the Tsuji reference cited by

the Examiner does not teach each and every element of Applicant's invention, as claimed in claim 26, as amended. Consequently, Tsuji does not anticipate claim 26, as amended, of Applicant's invention.

Applicant has canceled claim 27 without prejudice.

Applicant has amended claim 28. Claim 28 is dependent on claim 26, as amended, and, thus, is also not anticipated by Tsuji.

In view of the foregoing, Applicant respectfully requests the Examiner to withdraw the rejections to claims 26 and 28 under 35 U.S.C. § 102 (b).

Claim Rejections 35 U.S.C. § 102 (e)

Claims 1, 6-7, and 10-13

The Examiner has cited Takeda et al. (JP 05-013418), but Applicant believes that the Examiner intended to cite Fukuda et al. (JP 05-013418) so Applicant will respond accordingly below.

The Examiner has rejected claims 1, 6-7, and 10-13 under 35 U.S.C. § 102 (e) as being anticipated by Fukuda et al. (JP 05-013418).

Applicant respectfully disagrees with the Examiner. Applicant has amended claim 1. Claim 1, as amended, claims a device having Input/Output (I/O) connections to a package or board comprising: a bond pad (21B); vias (22N, 22N) located over the bond pad; a BLM (24) located over the vias, the BLM split into two or more segments (24N, 24N), the segments in close proximity to each other, the segments separated by a gap (23); and a bump (25) located directly on the segments. See Figures 2a-2b. Also, see lines 17-31 on page 6 and lines 1-4 on page 7 of the specification.

In contrast, the Fukuda et al. reference cited by the Examiner teaches a bond pad (3), vias (areas between layers 4 and 5) located over the bond pad, a BLM located over the bond pad, the BLM having segments in close proximity, separated by gaps, and electrically connected to the vias, a Cu-plated layer (8) over each segment, and a solder bump (9) over all the Cu-plated layers. See Figures 4-6.

However, the Fukuda et al. reference does not teach a solder bump located directly on the segments. Thus, the Fukuda et al. reference cited by the Examiner does not teach each and every element of Applicant's invention, as claimed in claim 1, as amended. Consequently, Fukuda et al. does not anticipate claim 1, as amended, of Applicant's invention.

Claims 6-7 and 10-13 are dependent on claim 1, as amended, and, thus, are also not anticipated by Fukuda et al.

In view of the foregoing, Applicant respectfully requests the Examiner to withdraw the rejections to claims 1, 6-7, and 10-13 under 35 U.S.C. § 102 (e).

Claim Rejections 35 U.S.C. § 103 (a)

Claims 2-4

The Examiner has cited Takeda et al. (JP 05-013418), but Applicant believes that the Examiner intended to cite Fukuda et al. (JP 05-013418) so Applicant will respond accordingly below.

The Examiner has rejected claims 2-4 under 35 U.S.C. §103 (a) as being unpatentable over Fukuda et al. (JP 05-013418) and Tadauchi et al. (US 6,464,122).

Applicant respectfully disagrees with the Examiner. Claims 2-4 are dependent on claim 1, as amended. Claim 2 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the bump (25) includes a Lead-Tin (Pb-Sn) solder. Claim 3 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the bump (25) is free of Lead (Pb). Claim 4 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the bump (25) includes a Tin-Silver-Copper (Sn-Ag-Cu) ternary alloy.

Claim 1, as amended, claims a device having Input/Output (I/O) connections to a package or board comprising: a bond pad (21B); vias (22N, 22N) located over the bond pad; a BLM (24) located over the vias, the BLM split into two or more segments (24N, 24N), the segments in close proximity to each other, the segments separated by a gap (23); and a bump (25) located directly on the segments. See Figures 2a-2b. Also, see lines 17-31 on page 6 and lines 1-4 on page 7 of the specification.

In contrast, the Fukuda et al. reference cited by the Examiner teaches a bond pad (3), vias (areas between layers 4 and 5) located over the bond pad, a BLM located over the bond pad, the BLM having segments in close proximity, separated by gaps, and electrically connected to the vias, a Cu-plated layer (8) over each segment, and a solder bump (9) over all the Cu-plated layers. See Figures 4-6.

However, the Fukuda et al. reference does not teach a solder bump located directly on the segments. Tadauchi et al. teaches a solder containing lead. See Col. 9, line 51. Thus, a combination of Fukuda et al. and Tadauchi et al. would still not produce Applicant's invention, as claimed in claims 2-4. Consequently, Applicant's invention, as claimed in claims 2-4 would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the two references cited by the Examiner do not teach, suggest, or render obvious claims 2-4 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejection to claims 2-4 under 35 U.S.C. §103 (a).

Claims 5 and 8-9

The Examiner has cited Takeda et al. (JP 05-013418), but Applicant believes that the Examiner intended to cite Fukuda et al. (JP 05-013418) so Applicant will respond accordingly below.

The Examiner has rejected claims 5 and 8-9 under 35 U.S.C. §103 (a) as being unpatentable over Fukuda et al. (JP 05-013418) and Wark et al. (US 6.613,662).

Applicant respectfully disagrees with the Examiner. Claims 5 and 8-9 are dependent on claim 1, as amended. Claim 5 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the bump includes an Electrically Conductive Adhesive (ECA). Claim 8 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the BLM includes a lower layer and an upper layer and wherein the lower layer includes Titanium (Ti) with a thickness of about200 to 1500 Angstroms. Claim 9 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the BLM includes a lower layer and an upper layer and wherein the upper layer includes Nickel-Vanadium (Ni-V) with a thickness of about 1000 to 8000 Angstroms.

Claim 1, as amended, claims a device having Input/Output (I/O) connections to a package or board comprising: a bond pad (21B); vias (22N, 22N) located over the bond pad; a BLM (24) located over the vias, the BLM split into two or more segments (24N, 24N), the segments in close proximity to each other, the segments separated by a gap (23); and a bump (25) located directly on the segments. See Figures 2a-2b. Also, see lines 17-31 on page 6 and lines 1-4 on page 7 of the specification.

Wark et al. teaches a bump but does not teach any vias. Thus, a combination of Fukuda et al. and Wark et al. would still not produce Applicant's invention, as

claimed in claims 5 and 8-9. Consequently, Applicant's invention, as claimed in claims 5 and 8-9, would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the two references cited by the Examiner do not teach, suggest, or render obvious claims 5 and 8-9 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejection to claims 5 and 8-9 under 35 U.S.C. §103 (a).

Claims 14-15

The Examiner has cited Takeda et al. (JP 05-013418), but Applicant believes that the Examiner intended to cite Fukuda et al. (JP 05-013418) so Applicant will respond accordingly below.

The Examiner has rejected claims 14-15 under 35 U.S.C. §103 (a) as being unpatentable over Fukuda et al. (JP 05-013418) and Wong (US 6,577,017).

Applicant respectfully disagrees with the Examiner. Applicant has amended claim 1. Claim 1, as amended, claims a device having Input/Output (I/O) connections to a package or board comprising: a bond pad (21B); vias (22N, 22N) located over the bond pad; a BLM (24) located over the vias, the BLM split into two or more segments (24N, 24N), the segments in close proximity to each other, the segments separated by a gap (23); and a bump (25) located directly on the segments. See Figures 2a-2b. Also, see lines 17-31 on page 6 and lines 1-4 on page 7 of the specification.

Wong teaches a single via, but does not teach a bump. Thus, a combination of Fukuda et al. and Wong would not produce Applicant's invention, as claimed in claims 14-15. Consequently, Applicant's invention, as claimed in claims 14-15, would

not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the two references cited by the Examiner do not teach, suggest, or render obvious claims 14-15 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejection to claims 14-15 under 35 U.S.C. §103 (a).

Conclusion

Applicant believes that all claims pending are now in condition for allowance so such action is earnestly solicited at the earliest possible date.

PETITION FOR EXTENSION OF TIME
PURSUANT TO 37 C.F.R. § 1.136 (a)

Applicant respectfully petitions pursuant to 37 CFR 1.136(a) for a two-month extension of time to file this response to the Office Action mailed April 14, 2004. The extended period is set to expire on Tuesday, September 14, 2004. A check in the amount of $420.00 is enclosed to cover the fee for a two-month extension of time.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time.

Should there be any additional charge or fee, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, please charge Deposit Account No. 02-2666.

If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact the undersigned at (408) 720-8300.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: September 14, 2004

George Chen
Reg. No. 50,807

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

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